

## CLAIMS

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

- 1                   1. A dual port SRAM cell comprising six nMOS devices,  
2                   two nMOS pull-down devices,  
3                   two nMOS first pair of transfer devices,  
4                   two nMOS second pair of transfer devices,  
5                   a first pair of bitlines coupled to the drains of the first pair of transfer  
6 devices,  
7                   a second pair of bitlines coupled to the drains of the second pair of  
8 transfer devices,  
9                   a first wordline coupled to the gates of the first pair of transfer devices,  
10                  and  
11                  a second wordline coupled to the gates of the second pair of transfer  
12 devices.
- 1                   2. The dual port SRAM cell of claim 1, wherein said first pair of  
2 transfer gates also serve as the load devices for the SRAM cell.
- 1                   3. The dual port SRAM cell of claim 1, wherein said second pair of  
2 transfer gates also serve as the load devices for the SRAM cell.
- 1                   4. The dual port SRAM cell of claim 1, wherein said first wordline is  
2 the first port for read and write operations.
- 1                   5. The dual port SRAM cell of claim 1, wherein said second wordline is  
2 the second port for read and write operations.

1 6. A dual port SRAM cell comprising four nMOS and three pMOS  
2 devices,  
3 two nMOS pull-down devices,  
4 two pMOS pull-down devices,  
5 two nMOS first pair of transfer devices,  
6 one pMOS second transfer device,  
7 a first pair of bitlines coupled to the drains of the first pair of transfer  
8 devices,  
9 a second bitline coupled to the drain of the second transfer device,  
10 a first wordline coupled to the gates of the first pair of transfer devices,  
11 and  
12 a second wordline coupled to the gate of the pMOS second transfer  
13 device.

1 7. The dual port SRAM cell of claim 6, wherein said first wordline is  
2 the first port for read and write operations.

1 8. The dual port SRAM cell of claim 6, wherein said second wordline is  
2 the second port for read-only operations.

1 9. A high-speed SRAM architecture comprising:  
2 two dual port SRAM blocks,  
3 a TAG cache, and  
4 an interface circuit.

1                   10. The high-speed SRAM architecture of claim 9, wherein a write  
2 operation is performed with a first  $\frac{1}{2}$  cycle writing data to the first dual port cache, and  
3 a second  $\frac{1}{2}$  cycle writing data to the second dual port cache via the read-write port.

1                   11. The high-speed SRAM architecture of claim 9, wherein a read  
2 operation is performed with a first  $\frac{1}{2}$  cycle reading data from the first dual port cache,  
3 and a second  $\frac{1}{2}$  cycle reading data from the second dual port cache via either of the  
4 dual ports.

1                   12. The high-speed SRAM architecture of claim 9, wherein the  
2 addresses of valid data stored in the dual dual-port SRAM cache are stored in the TAG  
3 cache, incoming addresses are compared to addresses stored in the TAG and to  
4 schedule read and write operations, and when new data is stored in the dual dual-port  
5 cache, the status in the TAG cache is updated.